Serial No.: 10/092,372

REMARKS

Claims 1-29 are pending in the application. Claims 2-25 and 27-29 have been amended herein. Favorable reconsideration of the application is respectfully requested.

I. ALLOWABLE SUBJECT MATTER

Applicants acknowledge with appreciation the indicated allowability of claims 16-19, 21-23 and 25. These claims will be in condition for allowance upon being amended to independent form.

II. REJECTION OF CLAIMS 2-25 AND 27-29 UNDER 35 USC §112, 2ND

Claims 2-25 and 27-29 stand rejected under 35 USC §112, second paragraph, based on the informalities noted in ¶1-4 of the Office Action.

Applicants have amended claims 2-25 and 27-29 to correct the informalities. Accordingly, applicants respectfully submit that claims 2-25 and 27-29 clearly define applicants' invention. Withdrawal of the rejection is respectfully requested.

III. REJECTION OF CLAIMS 1-3, 13-15, 20, 24 AND 26-29 UNDER 35 USC §102(e)

Claims 1-3, 13-15, 20, 24 and 26-29 stand rejected under 35 USC §102(e) based on *Eglit*. This rejection is respectfully traversed for at least the following reasons.

As described in more detail below, *Eglit* discloses a display controller in which *N of every N+1* source image frames are used for generating display signals. The $(N+1)^{st}$ source image frame may be ignored. The present invention, in contrast, supplies an enable signal *each N^{th} frame*, as recited in claim 1.

More particularly, claim 1 describes a controller for controlling the frame refresh rate of an active matrix display in accordance with the present invention. The controller includes a first circuit responsive to display signals from a display controller *for*

supplying an enable signal (FE) for each Nth frame, where N is an integer greater than zero and is selectable from a plurality of values. In addition, the controller includes a second circuit for enabling refreshing of the display by each Nth frame supplied to the display controller in response to the enable signal (FE). Moreover, the second circuit *prevents refreshing of the display by each other frame* supplied to the display controller in the absence of the enable signal (FE).

For example, during a frame rate reduction period (e.g., FRC is at logic high-See Fig. 3 of Application), the controller according to claim 1 provides an enable signal FE (e.g., logic high) each Nth frame, and does not provide an enable signal FE (e.g., logic low) for the frames not corresponding to the Nth frame. Thus, if N is 4, then every fourth frame the enable signal FE will be set to logic high, while during the remaining 3 frames, the enable signal will be set to logic low. Therefore, during the four frame period, the enable signal FE is only provided during one frame.

Eglit is discussed in the present application beginning at page 5. *Eglit* describes a display unit in which N of every N+1 source image frames are used for generating display signals; that is, for refreshing a display screen. The $(N+1)^{st}$ source image frame is ignored. (see, e.g., col. 3, lines 57-59) As is described in *Eglit* with respect to Fig. 4, an inverter 470 provides a write-enable signal having a logical high value for the first N source image frames and a low value during the $(N+1)^{st}$ source image frame.

In other words, *Eglit* describes a display unit in which the display rates may be varied only slightly. In *Eglit*, all the frames provide a refreshing of the display *except* for the $(N+1)^{st}$ frame. (see, e.g., col. 9, lines 16-30).

The present invention relates to a controller in which an enable signal is provided for each Nth frame such that a second circuit enables a refreshing of the display *only* by each Nth frame. The second circuit prevents refreshing of the display by each other frame supplied to the display controller. (see, e.g., specification, pg. 29, lines 7-9).

Describing *Eglit* in more detail, the reference teaches that the cycle counter 430 (Fig. 4) counts the number of source image frames as VSYNC provides the clock signal. The output of cycle counter 430 is provided as an input to comparator 460, which compares the value of N with the output of the counter. When the $(N+1)^{st}$ frame is being received, the two inputs have equal values and the output of comparator 460 is at a logical value 1 during the entire frame. (Col. 9, lns. 16-23). Thus, the write enable signal, which is derived by inverting the output of the comparator 460, is at logic 0 during the entire $(N+1)^{st}$ frame.

For example, if N is 4 as in the example above, the output of the comparator 460 will be at logic 1 every 5^{th} frame (4+1=5), and at logic 0 for the remaining frames. Thus, the write enable signal 479 is at logic 1 (i.e., enabled) for the first four frames, and disabled for the fifth frame (the 5^{th} frame is ignored). Clearly, this is not equivalent to the present invention, wherein every Nth frame the enable signal FE is set to logic high, while during the remaining frames the enable signal is set to logic low.

Thus, *Eglit* describes a display unit in which the display rates may be varied only slightly. In *Eglit*, all the frames provide a refreshing of the display except the $(N+1)^{th}$ frame.

Accordingly, *Eglit* does not teach or suggest a controller for controlling the frame refresh rate of an active matrix display, including a first circuit responsive to display signals from a display controller for supplying an enable signal (FE) for each Nth frame, where N is an integer greater than zero and is selectable from a plurality of values, as recited in claim 1.

Withdrawal of the rejection of claims 1-3, 13-15, 20, 24 and 26-29 is respectfully requested.

Serial No.: 10/092,372

IV. REJECTIONS OF CLAIMS 4 AND 5-12 UNDER 35 USC §103(a)

Claim 4 stands rejected under 35 USC §103(a) based on *Eglit* in view of *Kawasaki et al.* Claims 5-12 are rejected under 35 USC §103(a) based on *Eglit* in view of *Atkinson*.

Claims 4 and 5-12 each depend from claim 1 either directly or indirectly. Therefore, these claims may be distinguished over the teachings of *Eglit* for at least the same reasons discussed above in relation to claim 1. Furthermore, *Kawasaki et al.* and *Atkinson* do not make up for the above-discussed deficiencies in *Eglit*.

As a result, withdrawal of the rejections is respectfully requested.

V. CONCLUSION

Accordingly, all claims 1-29 are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Serial No.: 10/092,372

Should a petition for an extension of time be necessary for the timely reply to the outstanding Office Action (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

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